In the specification, please delete both paragraphs of the Abstract on page 33 and insert the following paragraph therefor:

--An apparatus to perform no-latency conditional branching has a sequencer for executing program instructions including one or more conditional branch instructions. The conditional branch instruction is a binary word specifying a branch condition address and a conditional instruction. The branch unit has a programmable flag selection memory and a plurality of first flag selectors and determines in hardware whether to branch according to the conditional instruction. Each first flag selector accepts a plurality of available flags and selects a flag based upon contents in the flag selection memory. A second flag selector accepts the flags from the first flag selectors and selects one of the flags to present as a branch flag based upon the branch condition address. The branch flag indicates whether to branch to the destination address.--